EMBEDDED SYSTEMS-II

(Professional Elective-VI)/ (Common for CSE,IT)

COURSE CODE: 15CT1136 **L T P C**
3 0 0 3

Pre-requisites: Electronics Devices and Circuits, Computer Organization.

COURSE OUTCOMES:
At the end of the course the student shall be able to

CO1: Understand the ARM processor architecture
CO2: Understand ARM Instruction set
CO3: Develop optimized programs for ARM processor
CO4: Use interrupt handling techniques in ARM Applications
CO5: Describe ARM memory management units

UNIT-I **(8-10 Lectures)**

ARM EMBEDDED SYSTEMS

The RISC Design Philosophy, The ARM Design Philosophy, Embedded System Hardware, Embedded System Software.

ARM PROCESSOR FUNDAMENTALS

Registers, Current Program Status Register, Pipeline, Exceptions, Interrupts, and the Vector Table**(TEXT BOOK-1)**

UNIT-II **(8-10 Lectures)**

THE ARM INSTRUCTION SET

Introduction, Exceptions, Conditional execution, Branch and Branch with Link (B, BL), Branch, Branch with Link and eXchange (BX, BLX), Software Interrupt (SWI),Data processing instructions, Multiply instructions,Count leading zeros (CLZ - architecture v5T only),Single word and unsigned byte data transfer instructions, Half-word and signed byte data transfer instructions, Multiple register transfer instructions, Swap memory and register instructions (SWP),Status register to general register transfer instructions ,General register to status register transfer instructions**(TEXT BOOK-2)**

UNIT-III **(8-10 Lectures)**

WRITING AND OPTIMIZING ASSEMBLY CODE

Profiling and Cycle Counting: Instruction Scheduling, Scheduling of Load Instructions, Register Allocation: Allocating Variables to Register Numbers, Using More than 14 Local Variables: Making the Most of Available Registers, Conditional Execution: Looping Constructs: Decremented Counted Loops, Unrolled Counted Loops, Multiple Nested Loops, Other Counted Loops, Bit Manipulation: Fixed-Width Bit-Field Packing and Unpacking, Variable-Width Bitstream Packing, Variable-Width Bitstream Unpacking**(TEXT BOOK-1)**

UNIT-IV **(8-10 Lectures)**

EXCEPTION AND INTERRUPT HANDLING

Exception Handling, Interrupts , Interrupt Handling Schemes: non-nested interrupt handler, **Firmware:** Firmware and Bootloader

EMBEDDED OPERATING SYSTEMS : Fundamental components

(**TEXT BOOK-1)**

UNIT-V **(8-10 Lectures)**

MEMORY MANAGEMENT UNITS

Moving from an MPU to an MMU, How Virtual Memory Works, Details of the ARM MMU, Page Tables, The Translation Lookaside Buffer, Domains and Memory Access Permission, The Caches and Write Buffer.(**TEXT BOOK-1)**

TEXT BOOKS:

1. Andrew N. Sloss, Dominic Symes, Chris Wright, "*ARM System Developer's Guide: Designing and Optimizing System Software*", 1st Edition, ELSEVEIR and MORGAN KAUFMANN Publishers,2008
2. Steve Furber, "*ARM System-on-Chip Architecture*", 2nd edition, Addison-Wesley Professional, 2000

REFERENCES:

1. Bendapudy Kanta Rao, "*Embedded Systems*" , Prentice Hall India", 1 st Edition, 2011.
2. David Seal , "ARM Architecture Reference Manual", 2nd edition, Addison-Wesley Professional, 2000

WEB REFERENCES:

http://www.nptel.iitm.ac.in/video.php?subjectId=108102045